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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION N
10/781,759	02/20/2004	Takaaki Higashida	2004-0276	3778
513	7590	10/18/2004	EXAMINER	
WENDEROTH, LIND & PONACK, L.L.P.			NGUYEN, DONGHAI D	
2033 K STREET N. W.			ART UNIT	
SUITE 800			PAPER NUMBER	
WASHINGTON, DC 20006-1021			3729	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/781,759	Applicant(s) HIGASHIDA ET AL.	
	Examiner Donghai D. Nguyen	Art Unit 3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 08/890,009.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2/20/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase “by a flip-chip mounting process” (claim 1, line 13) is vague and indefinite since it is unclear how the process is carried out and what exact step(s) is actually involved in the “flip-chip mounting process”.

The phrase “plastic treatment” (claim 9, line 4) is vague and indefinite. It is unclear as to what process/step is performed in treating the plastic.

The phrases “machining” (claim 11, line 2) and “machining at ... the injecting” (claim 13, lines 2-3) are vague and indefinite since it is unclear as to the exact step(s) (i.e., grinding, punching, etc.) is carried out.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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4. Claims 1, 2, 4, 8, 9, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 4,616,406 to Brown.

Regarding claims 1 and 12, Brown discloses a method for manufacturing a semiconductor element-mounting board, comprising: arranging a plurality of conductive members (14) in a mold (20); and injecting the resin material (12) into the mold after the conductive members are arranged therein so that the conductive members and the resin material are integrally molded to form a base member (See fig. 4) having a semiconductor element-mounting face (top surface) and a circuit board-mounting face opposite the semiconductor element-mounting face (bottom surface in Fig. 4), the arranging of the conductive members comprising orienting the conductive members in the mold so that the conductive members are substantially orthogonal to the semiconductor element-mounting face and the circuit board-mounting face and extend linearly through an interior of the base member between the semiconductor element-mounting face and the circuit board-mounting face (Fig. 1); mounting and electrically connecting a semiconductor element (10) to the semiconductor element-mounting face by a flip-chip mounting process (col. 5, lines 30-33; Fig. 4); and mounting and electrically connecting the circuit board-mounting face to a circuit board (col. 4, lines 60-64).

Regarding claims 2 and 4, Brown discloses a wiring (by printing and heating/reflow solder paste) on the semiconductor element-mounting face and the circuit board-mounting face (Col. 4, lines 39-42 and Col. 4, lines 67-68).

Regarding claim 8, see Col. 4, lines 48-51.

Regarding claims 9 and 13, see Fig. 4 and col. 4, lines 51-52.

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5. Claims 1-3, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by JP Application No. 03006749 to Dotani.

Regarding claims 1, and 12, Dotani discloses a method for manufacturing a semiconductor element-mounting board, comprising: arranging a plurality of conductive members (1) in a mold (23); and injecting the resin material (11/21) into the mold after the conductive members are arranged therein so that the conductive members and the resin material are integrally molded to form a base member (Figs. 1 and 5C) having a semiconductor element-mounting face and a circuit board-mounting face opposite the semiconductor element-mounting face (Fig. 5C), the arranging of the conductive members comprising orienting the conductive members in the mold so that the conductive members are substantially orthogonal to the semiconductor element-mounting face and the circuit board-mounting face and extend linearly through an interior of the base member between the semiconductor element-mounting face and the circuit board-mounting face (Fig. 5A); mounting and electrically connecting a semiconductor element (15A) to the semiconductor element-mounting face by a flip-chip mounting process; and mounting and electrically connecting the circuit board-mounting face to a circuit board (15B in Figs. 4).

Regarding claims 2 and 3, Fig 5D shows forming the wiring pattern (13) on both faces of the base member.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Brown or Dotani in view of JP Application No. 60-078366 to Furukawa et al.

Both Brown and Dotani disclose the all the claimed invention of forming a bas member except roughing or applying adhesive agent to the circumferential surface of the conductor member. Furukawa et al teach the step of roughing or applying adhesive agent to the circumferential surface of the conductor member for increasing adhesive strength between conductor member and resin (Purpose and Constitution sections). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify either Brown or Dotani to have a step of roughing or applying adhesive agent to the circumferential surface of the conductor member as taught by Furukawa et al for increasing adhesive strength between conductor member and resin.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Brown or Dotani in view of US Patent 5,165,651 to Welch et al.

Both Brown and Dotani disclose the all the claimed invention of forming a bas member except injecting the resin material in an axial direction parallel to the longitudinal of the conductive member. Welch et al teach injecting the resin material (50) in an axial direction parallel to the longitudinal of the conductive member (32V/34) through two symmetrical injection openings (20) for forming a fortified structure. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify either Brown or Dotani to

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inject the resin material in an axial direction parallel to the longitudinal of the conductive member through two symmetrical injection openings as taught by Welch for forming a fortified structure.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over either Brown or Dotani in view of US Patent No. 4,778,950 to Lee et al.

Both Brown and Dotani disclose the all the claimed invention of forming a base member except cutting the base member block molded in a direction orthogonal to the longitudinal axes of the conductive member. Lee et al cutting the base member block molded (20 Fig. 4) in a direction orthogonal to the longitudinal axes of the conductive member (14 Fig. 5) for forming a base member having individual conductive members uniformly dispersed (Col. 6, lines 50-57). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify either Brown or Dotani to have the base member block molded cuts in a direction orthogonal to the longitudinal axes of the conductive member as taught by Lee et al for forming a base member having individual conductive members uniformly dispersed.

Allowable Subject Matter

10. Claims 7, 10, and 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

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Conclusion

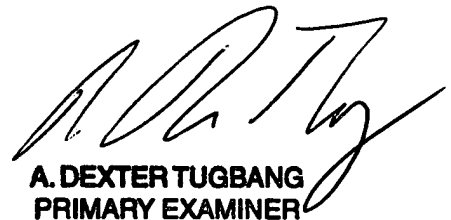
11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghai D. Nguyen whose telephone number is (703) 305-7859. The examiner can normally be reached on Monday-Friday (9:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter D. Vo can be reached on (703) 308-1789. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DN


A. DEXTER TUGBANG
PRIMARY EXAMINER